UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/782,782 | 02/23/2004 | Don-Woo Lee | SEC.1143 | 5510 |

20987 7590 06/27/2005

VOLENTINE FRANCOS, & WHITT PLLC
ONE FREEDOM SQUARE
11951 FREEDOM DRIVE SUITE 1260
RESTON, VA 20190

| EXAMINER | |
|---|---|
| SARKAR, ASOK K | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2891 | |

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/782,782 | LEE ET AL. | |
| | Examiner | Art Unit | |
| | Asok K. Sarkar | 2891 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-20* is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *1-3 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claims 1 – 3 and 13 are objected to because of the following informalities: In claim 1, starting in line 5 following the phrase, "... on the substrate," the phrase "including over the conductive layer" should be changed to "covering the conductive layer" or "over the conductive layer". Appropriate correction is required.

In claim 2, in line 3 following the phrase, "... on the substrate," the phrase "including over the conductive layer" should be changed to "covering the conductive layer" or "over the conductive layer". Appropriate correction is required.

In claim 3, in line 3 following the phrase, "... on the substrate," the phrase "including over the conductive layer" should be changed to "covering the conductive layer" or "over the conductive layer". Appropriate correction is required.

In claim 13, in line 4 following the phrase, "... on the substrate," the phrase "including over the structure" should be changed to "covering the structure" or "over the structure". Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Gray, US 4,964,946.

Regarding claim 1, Gray teaches a method of forming a conductive pattern of a device, comprising:

- forming a conductive layer 10 on a substrate such that the conductive layer protrudes above an upper surface of the substrate (see Fig. 1A);
- forming a polishing protection layer 12 on the substrate, over the conductive layer, whereby the polishing protection layer presents a step between a portion of the polishing protection layer lying directly over the substrate and a portion of the polishing layer lying over the conductive layer (see Fig. 1B);
- forming a step compensation layer 14 on the polishing protection layer that reduces the step presented by the polishing protection layer 12 (see Fig. 1C);
- removing portions of the step compensation layer and the polishing protection layer to expose the conductive layer and etching away part of the exposed conductive layer to form a conductive pattern on the substrate (see Fig. 1G) in column 2, lines 9 – 65.

Regarding claims 2 and 3, Gray teaches the polishing protection layer comprises forming silicon nitride layer on the substrate, over the conductive layer in column 2, lines 22 – 28.

Regarding claims 4 – 6, Gray teaches forming of the step compensation layer comprises forming a layer of silica that is inherently reflowable on the polishing protection layer that is formed using tetra ethyl ortho silicate by a chemical vapor deposition process in column 2, lines 29 – 33.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 7 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Gray, US 4,964,946 in view of Wolf, "Silicon processing for the VLSI Era, Vol. 2, p 238 (1990), Lattice Press, CA.

Regarding these claims, Gray teaches etching the various layers deposited on the conductive layer in between column 2, line 58 and column 3, line 13, but fails to teach various stages of etching such as first planarization process (claim 7), etch-back process (claim 8), second planarization process (claim 9), chemical mechanical polishing (claim 10), removing the remaining layers from around the conductive pattern (claim 11) by wet etching with phosphoric acid (claim 12).

Wolf teaches that a CMP process together with an etch-back process can be very effective in rapidly planarizing elevated surface features without significantly affecting the flat areas on the substrate under the heading "Chemical Mechanical Polishing" in page 238.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Gray and expose the protruding conductive feature on the substrate by the planarization process combining CMP process together with an etch-back process for the benefit of rapid removal of layers as taught by Wolf in page 238 and then remove the extra polishing protection layer around the conductive pattern by a wet etching process for the benefit of better selectivity between the polishing protection layer and the conductive feature. For silicon nitride as the polishing protection layer, phosphoric acid is a well-known etchant.

***Allowable Subject Matter***

8. Claims 13 – 20 are allowed.

9. The following is an examiner's statement of reasons for allowance:

Claims 13 – 20 recite, inter alia, a method of manufacturing a non-volatile semiconductor memory device comprising the steps of forming a conductive layer over a floating gate structure on a substrate, forming a polishing protection layer on the conductive layer, forming a step compensation layer on the polishing protection layer and removing portions of the step compensation layer and the polishing protection layer to expose the conductive layer. Chern, US 6,706,592 teaches a method of manufacturing a non-volatile semiconductor memory device, but he fails to teach forming a step compensation layer on the polishing protection layer formed on the conductive layer. Additionally, the art of record does not disclose or anticipate the above limitation in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

***Conclusion***

10. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok K. Sarkar
June 21, 2005

Primary examiner